Replacement claim 21:

C6

21. (Amended) The device according to claim 12, wherein said pattern of circuit connections includes at least one of the following to interconnect said plurality of circuit devices: a signal plane, a power plane and a ground plane.

REMARKS

This Amendment and Response is filed in reply to the Office Action dated November 20, 2002. The issues presented in the November 20, 2002 Office Action are addressed below.

The Draftsperson objected to Figures 1-7 under 37 C.F.R. 1.84(g) and 37 C.F.R. 1.84(i). Formal drawings are submitted with this Amendment.

The Examiner objected to the amendment filed January 8, 2002 under 35 U.S.C. § 132 as introducing new matter into the disclosure, contending that the added material "the decoupling capacitor 14 may be connected in parallel with the power plane 28 and the ground plane 29" was not supported in the original disclosure.

The Examiner rejected claim 22 under 35 U.S.C. § 112 as containing subject matter not described in the specification in such as way as to reasonably convey to one of skill in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention, contending that the phrase "wherein said decoupling capacitor connects in parallel between said power and ground planes" is not described in the specification and not shown in the figures in the original disclosure.

The Examiner rejected claims 12, 21, 23, 30, 32 and 33 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. (JP 406,295,981A). The Examiner rejected claims 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. in view of Tuckerman (U.S. Patent No. 5,274,270). The Examiner rejected claims 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. in view of Smith (U.S. Patent No. 4,890,192) and rejected claim 31 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. in view of Eichelberger (U.S. Patent No. 5,841,193).

Applicant traverses the Examiner's rejections and respectfully requests reconsideration in view of the amendments and remarks.

With respect to the Examiner's objection to the amendment filed January 8, 2002 under 35 U.S.C. § 132, Applicants submit that Fig. 2 shows a decoupling capacitor 14 connected in parallel with the power plane 31 and the ground plane 33. Applicants regret any confusion based on Applicants' previous amendment to the specification, which indicated the capacitor 14 may be connected in parallel with its power plane 28 and its ground plane 29. One skilled in the art can readily recognize from Fig. 2, as originally filed and as filed herewith in the formal drawings, that the power plane 28 and the ground plane 29 of capacitor 14 are connected in parallel with the power plane 31 and the ground plane 33 of the interconnecting layer 16. Thus, the matter introduced with the amendment provided herein is clearly supported by Fig. 2 of the original disclosure. Applicants respectfully request that the objection to the amendment be withdrawn.

Additionally, amendments to the specification are provided herein to better comport the specification and figures. No new matter has been added. In the paragraph beginning on page 8, line 22, the use of ceramic for the support base is supported in the background of the specification, e.g., page 2, line 2. Amendments to the paragraph beginning on page 9, line 8, are discussed above. Amendments to the paragraph beginning on page 9, line 23 and the paragraph beginning on page 10, line 18, clarify the wording of the descriptions therein.

With respect to the Examiner's rejection of claim 22 under 35 U.S.C. § 112, Applicants submit that the language of the claim is fully supported by Fig. 2, as described above. In addition, the claim is supported by the amendment to the specification provided herein, which in turn is supported by the original disclosure as described above. Based on the above, Applicants respectfully request reconsideration of the rejection of claim 22. There being no other rejections of claim 22, Applicants submit that claim 22 is in condition for allowance.

With respect to the rejections under 35 U.S.C. § 103(a), Takashi et al. describe a semiconductor device, wherein a PN junction protective diode is formed between the N-type diffusion layer 22 and the P-type Si wafer substrate 16 to protect a decoupling capacitor 24 within the device. The P-type Si wafer substrate is an active component of the semiconductor device, in that the diode is formed between the diffusion layer 22 and the substrate 16. In addition, the decoupling capacitor 24 is formed as part of the interconnecting layer 18 and is coupled to the diffusion layer 22, as indicated by connection 27. In contrast, Applicants provide a device for interconnecting a *plurality of circuit devices*. An interconnect layer having a pattern

of circuit connections is formed over discrete decoupling capacitors thereby embedding the decoupling capacitors within the interconnect layer. Circuit devices, such as the Takashi et al. semiconductor device, can be mounted to the surface of the interconnect layer and coupled to the decoupling capacitors through the circuit connections of the interconnect layer. The support base 12 simply provides a mounting surface for Applicants' device and is not an active component of the device.

In comparing the Takashi et al. semiconductor device to Applicants' device, the Examiner is attempting to compare distinct levels of circuits. Takashi et al. provide a semiconductor device that may include a component 13. The component 13 is electrically connected to the P-type Si wafer substrate, as indicated by connection 21. Thus, the P-type Si wafer substrate 16, interconnect layer 18 and component 13 form an integral semiconductor device. Particularly, the capacitor 24 is formed as part of the interconnect layer 18. Applicants describe such devices and their shortcomings (page 4, lines 1-9).

Applicants, on the other hand, recite a device that can interconnect a plurality of semiconductor, or circuit, devices. The circuit devices 20 are not electrically connected to the support base 12. The decoupling capacitors are separate components and the interconnect layer is formed *over* the decoupling capacitors (Figs. 4-7). The decoupling capacitors are *mounted on* a surface, such as support base 12. A filler can be deposited between the components mounted on the surface to provide mechanical support (page 13, lines 16-20), yet allowing for electrical connection to the pads of the decoupling capacitors. The interconnect layer 16 can then be *formed over* the decoupling capacitors.

Takashi et al. fail to disclose a *device for interconnecting a plurality of circuit devices* having *a decoupling capacitor mounted on a surface* and *an interconnect layer formed over said decoupling capacitor, whereby electrical connections of said decoupling capacitor are embedded within the interconnect layer and whereby circuit connections of the interconnect layer couple to the decoupling capacitor and the plurality of circuit devices*, as recited in claim 12. Based on the above, Applicants submit that claim 12 is patentable over Takashi et al. Claims 21, 22 and 24-33 depend directly or indirectly from claim 12 and are deemed in condition for allowance, at least by their dependency.

CONCLUSION

Based on the above Remarks, it is respectfully submitted that this application is in condition for allowance. Accordingly, allowance is requested. The claim amendments should in no way be construed to be an acquiescence to any of the rejections. The amendments to claims 12 and 21 are being made solely to expedite the prosecution of the above-identified application.

Applicant reserves the option to further prosecute the same or similar claims in the instant or subsequent patent applications. If there are any remaining issues or the Examiner believes that a telephone conversation with Applicant's attorney would be helpful in expediting the prosecution of this application, the Examiner is invited to call the undersigned at (617)832-1175.

Respectfully submitted,

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Marked-up version of specification:

Paragraph beginning at page 8, line 22

The support base 12 depicted in Figure 1 can be formed of ceramic, silicon, polycrystalline silicon or other suitable material. The support base 12 can be any shape or any size, and the actual configuration of the support base 12 will depend upon the application.

Paragraph beginning at page 9, line 8

Turning to Figure 2, one portion, section A, of the MCM module 10 depicted in Figure 1 is shown in greater detail. Specifically, Figure 2 presents an enlarged view of section A of the MCM module 10, and more specifically depicts [the support base 12 having disposed thereon] the decoupling capacitor 14 which is embedded within the interconnect layer 16. Figure 2 presents a cross-sectional view of this portion of the MCM device 10 which cross-sectional view illustrates that the MCM device 10 is a multilayer device. Figure 2 further shows that the decoupling capacitors 14 can be electrically coupled to the ground plane [29] 33 and power plane [28] 31 of the MCM module 10. [In certain exemplary embodiments, the decoupling capacitor 14 may be connected in parallel with the power plane 28 and the ground plane 29.] Figure 2 further depicts that the interconnect layer 16 can include a plurality of layers that can be organized into a pattern of circuit connections that can be employed for interconnecting the circuit devices 20 mounted to the surface 18 of the interconnect layer 16. Figure 2 further shows that the interconnect layer 16 can include power and ground connections, 31 and 33, that can provide power to the circuit devices 20 and which are decoupled by the decoupling capacitors 14. In certain exemplary embodiments, the decoupling capacitor 14 may be connected in parallel with the power plane 31 and the ground plane 33.

Paragraph beginning at page 9, line 23

Specifically, Figure 2 illustrates that the capacitors 14 can have pads 26 located on an upper surface of the capacitors 14. The pads 26 can provide contact points that are electrically connected to the power plane 28 and ground plane 29 that form capacitor 14. The interconnect layer 16 includes metal layers, such as the ground layer 33 and the power layer 31, that connect to these contact points and therefore extend the ground plane 29 and power plane 28 [into the

interconnect layer 16] of the capacitor 14. The metal layers can connect, optionally in almost a direct line, through the interconnect layer 16 and to the power and ground connections of the circuit devices 20. In this way, the MCM 10 can provide a reduced interconnect lead and a low inductance chip to decoupling capacitor connection.

Paragraph beginning at page 10, line 18

Figures 3A - 3B depict one particular embodiment of a decoupling capacitor 30 that can be employed with the MCM 10 depicted in Figure 1. The depicted decoupling capacitor 30 is a component that is mounted to the support base 12 before the interconnect layer 16 is formed. The decoupling capacitor 30 can comprise a thin film MCM-D technology fabricated device, and in particular can be formed by multi-layer thin film processing with copper or aluminum metallization and SiO_2 dielectric material fabricated on a silicon base[d substrate] as shown in Figure 2. One such capacitor and techniques for forming such a capacitor is generally described in the above referenced U.S. Patent 5,134,539.

Marked-up version of claims:

12. (Twice Amended) A device for interconnecting a plurality of circuit devices, comprising:

[a support base having a first surface;]

a decoupling capacitor mounted on a [said] first surface; and

an interconnect layer having a pattern of circuit connections and being formed over said decoupling capacitor, whereby electrical connections of said decoupling capacitor [is] are embedded within said interconnect layer and said interconnect layer is disposed between said decoupling capacitor and said plurality of circuit devices,

and whereby said pattern of circuit connections of said interconnect layer is coupled to said decoupling capacitor and [a] said plurality of circuit devices[mounted on a surface of said interconnect layer opposite said first surface of said support base].

21. (Amended) The device according to claim 12, wherein said pattern of circuit connections includes at least one of the following to interconnect said plurality of circuit devices: a signal plane, a power plane and a ground plane.